REMARKS

Amended Claims

Claims 1-2, 13-14 and 22 are amended herein.

Claims Not Addressed by Examiner

Applicant notes that claims 2-9 were never specifically rejected by the Examiner in the detailed office action, although they are listed as rejected in the office action summary sheet and claim 1, from which claims 2-9 depend, was specifically rejected. Applicant therefore assumes that they stand rejected and requests the Examiner's reasons for rejection of claims 2-9.

Applicant therefore submits that the Final Office Action was premature and requests that the Examiner withdraw the finality of the rejection and issue another Office Action since Applicant has not been afforded the opportunity to address any specific rejections of claims 2-9. *See,* MPEP §706, §706.07, §706.07(a) and (c)-(e), §707.07, §707.07(g) and (i) and 37 C.F.R. §1.104.

Claim Rejections Under 35 U.S.C. § 102

Claims 13, 14, 16 and 17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kolodny et al (U.S. Patent No. 4,785, 199). Applicant respectfully traverses this rejection and submits that claims 13, 14, 16 and 17, as amended, are allowable for at least the following reasons.

Applicant respectfully maintains that Kolodny et al. does not disclose a memory array wherein each cell of the array has a first and second field effect transistor (FET) that are of the same conductivity type (i.e., having both P-FET or both N-FET devices). *See, e.g.*, Kolodny et al., Figs. 1-3; Abstract; column 1, line 50 to column 2, line 15; column 3, lines 3-28; and column 4, lines 23-39. Applicant also continues to maintain that Kolodny et al. does not disclose a floating gate memory cell structure containing a first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance and where the first and second FETs are each formed on a

substrate material of a first conductivity type and have source/drain regions that are formed of material of a second conductivity type. *See, e.g.*, Kolodny et al., Figs. 1 and 3, Abstract, column 2, line 53 to column 3, line 37.

Applicant therefore respectfully maintains that Kolodny et al. does not teach or disclose a semiconductor memory having a memory array, wherein each memory cell of the memory array has a floating gate structure that is spaced apart from the source/drain/channel regions of a first FET in a first section by a first distance, and spaced apart from the source/drain/channel regions of a second FET of a second section by a second distance, wherein the first distance is less than the second distance and where the first and second FETs are of the same conductivity type. As such, Applicant submits that Kolodny et al. does not teach or disclose each and every element of the Applicant's claimed invention.

Claim 13, as amended, recites, in part, "an array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance and where the first and second FETs are each formed on a substrate material of a first conductivity type and have source/drain regions that are formed of material of a second conductivity type." As stated above, Kolodny et al. does not teach or disclose such a memory cell having a first and second adjacent field effect transistors (FETs) of the same conductivity type, which have a common floating gate. Therefore, Kolodny et al. does not teach or disclose all elements of claim 13.

Claim 14, as amended, recites, in part, "an array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance and where the first and second FETs are each formed on a substrate material of a first conductivity type and have source/drain regions that are formed of material of a second conductivity type." As stated above, Kolodny et al. does not teach or

disclose such a memory cell having a first and second adjacent field effect transistors (FETs) of the same conductivity type, which have a common floating gate. Therefore, Kolodny et al. does not teach or disclose all elements of claim 14.

Applicant respectfully contends that claims 13 and 14 have been shown to be patentably distinct from the cited reference. As claims 16 and 17 depend directly or indirectly from independent claim 13, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 13, 14, 16 and 17.

Claim Rejections Under 35 U.S.C. § 103

Claims 1, 9-12, 22, 25, 26 and 28-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koyama (U.S. Patent No.4,630,085). Applicant respectfully traverses this rejection and requests reconsideration of the claims. Applicant submits that claims 1, 9-12, 18, 22, 25, 26 and 28-32 are allowable for the following reasons.

Applicant respectfully maintains that Koyama discloses a single floating gate FET EPROM gate structure, wherein the floating gate is uniformly spaced from single source and a single drain that are formed beneath the single planar FET memory cell and are coupled to a first and second aluminum contacts (The Examiner's referenced first and second columnar structures, Koyama, elements 22, 23, 29 and 30 of Figure 4; and column 6, lines 37-59). *See, e.g.*, Koyama, Figs. 4 and 5, Abstract, column 6, line 37 to column 8, line 5.

The Applicant therefore respectfully maintains that Koyama does not teach or suggest a floating gate memory cell including a first columnar structure having two first source/drain regions and a spaced apart second columnar structure having two second source/drain regions with a floating gate structure interposed between the first columnar structure and the second columnar structure and spaced apart from the first and second structures, the floating gate being positioned closer to a selected one of the first and second columnar structures.

Claim 1, as amended, recites, in part, "an array having memory cells arranged in rows and columns for storing a desired logic state, each cell including a first columnar structure having two first source/drain regions and a spaced apart second columnar structure having two second source/drain regions with a floating gate structure interposed between the first columnar

structure and the second columnar structure and spaced apart from the first and second structures, the floating gate being positioned closer to a selected one of the first and second columnar structures." As stated above, Koyama does not teach or suggest such an array of memory cells, each cell including a first columnar structure having two first source/drain regions and a spaced apart second columnar structure having two second source/drain regions with a floating gate structure interposed between the first columnar structure and the second columnar structure and spaced apart from the first and second structures, the floating gate being positioned closer to a selected one of the first and second columnar structures. Therefore, Koyama does not teach or suggest all elements of claim 1.

Claim 22, as amended, recites, in part, "positioning a first columnar structure on a substrate having at least two source/drain regions formed in it; positioning a second columnar structure on the substrate having at least two source/drain regions formed in it, wherein the second columnar structure is spaced apart from the first columnar structure; forming a gate structure between the first structure and the second structure; and interposing a floating gate structure between the first structure and the gate structure and between the second structure and the gate structure, the floating gate structure being positioned closer to selected one of the first structure and the second structure." As stated above, Kolodny et al. does not teach or suggest a method of forming a memory device having a plurality of interconnected memory cells, each cell comprising a first columnar structure on a substrate having at least two source/drain regions formed in it and a second columnar structure on the substrate having at least two source/drain regions formed in it. Therefore, Kolodny et al. does not teach or suggest all elements of claim 22.

Applicant respectfully contends that claims 1 and 22 have been shown to be patentably distinct from the cited reference. As claims 9-12, 18, 25, 26 and 28-32 depend from and further define claims 1 and 22, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1, 9-12, 18, 22, 25, 26 and 28-32.

Claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kolodny et al. Applicant respectfully traverses this rejection and requests reconsideration of the claim. Applicant submits that claim 18 is allowable for the following reasons.

Applicant respectfully notes that, as stated above in regards to the rejection of independent claim 13 from which claim 18 depends, Kolodny et al. fails to teach or disclose a semiconductor memory having a memory array, wherein each memory cell of the memory array has a floating gate structure that is spaced apart from the source/drain/channel regions of a first FET in a first section by a first distance, and spaced apart from the source/drain/channel regions of a second FET of a second section by a second distance, wherein the first distance is less than the second distance and where the first and second FETs are of the same conductivity type. As such, Kolodny et al. fails to teach or disclose independent claim 13 and therefore does not teach or suggest all elements of claim 18.

Applicant respectfully contends that claim 13, as pending, has been shown to be patentably distinct from the cited reference. As claim 18 depends from and further define claim 13 it is also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claim 18.

Allowable Subject Matter

Claims 15, 19-21, 23-24 and 27 were allowed.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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Andrew C. Walseth
Reg. No. 43,234

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T 612 312-2200
F 612 312-2250